TOTEM Motherboard

Software-Defined Radio for nanosatellites

Datasheet

info@alen.space
+34 623 186 080
www.alen.space

info@alen.space
+34 623 186 080
www.alen.space

info@alen.space
+34 623 186 080
www.alen.space

1 Changelog

Table 1 - Changelog

Date	Revision	Author	Description
13/01/2018	1.0	ANV/BFA	First revision
04/12/2018	1.1	DNL	Format update
07/03/2019	1.2	DNL	Absolute Maximum Ratings System bus definition
14/06/2019	1.3	ANV	Style changed
18/02/2021	1.4	ANV/VMB	Power consumptions updated Cover picture updated Interfaces updated Font changed (Calibri)
20/04/2021	1.5	ANV	Update P3, P4 and P5 pinout / description to meet TOTEM motherboard v1.1 release

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2 Overview

TOTEM-Motherboard is a Software-Defined Radio for nanosatellites. It is based on a high-performance System-On-Chip (Xilinx Zynq-7000 series) and a wide frequency range RF transceiver (AD9364). A FSI-connector based interface allows to easily piggy-back a custom RF frontend or any frontend from Alén Space, making a full, clean and easy integration solution when it comes to room optimization.

2.1 Highlight Features

- Wideband transceiver
  - 70 MHz - 6 GHz
  - Up to 56 MHz bandwidth
  - 2 x TX and 3 x RX ports
- RF frontend as a piggyback board
- Multiple Interface
  - Ethernet, UART, JTAG, I2C, CAN
- Zynq-7020 SoC
  - Linux operating system
- 2x 4Gb DDR3L (1 GB or 512 MB with ECC)
- 8 Gb NAND Flash
- 4 Mb MRAM (SPI controlled)
- Physical properties
  - Dimensions : 89.3 mm x 93.3 mm
  - Mass: 130 g (with shieldings)
  - PC104 Space standard
- Power supply: 5V
- Operational temperature: -40ºC to 85 ºC

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2.2 Block Diagram

2.2.1 TOTEM-Motherboard

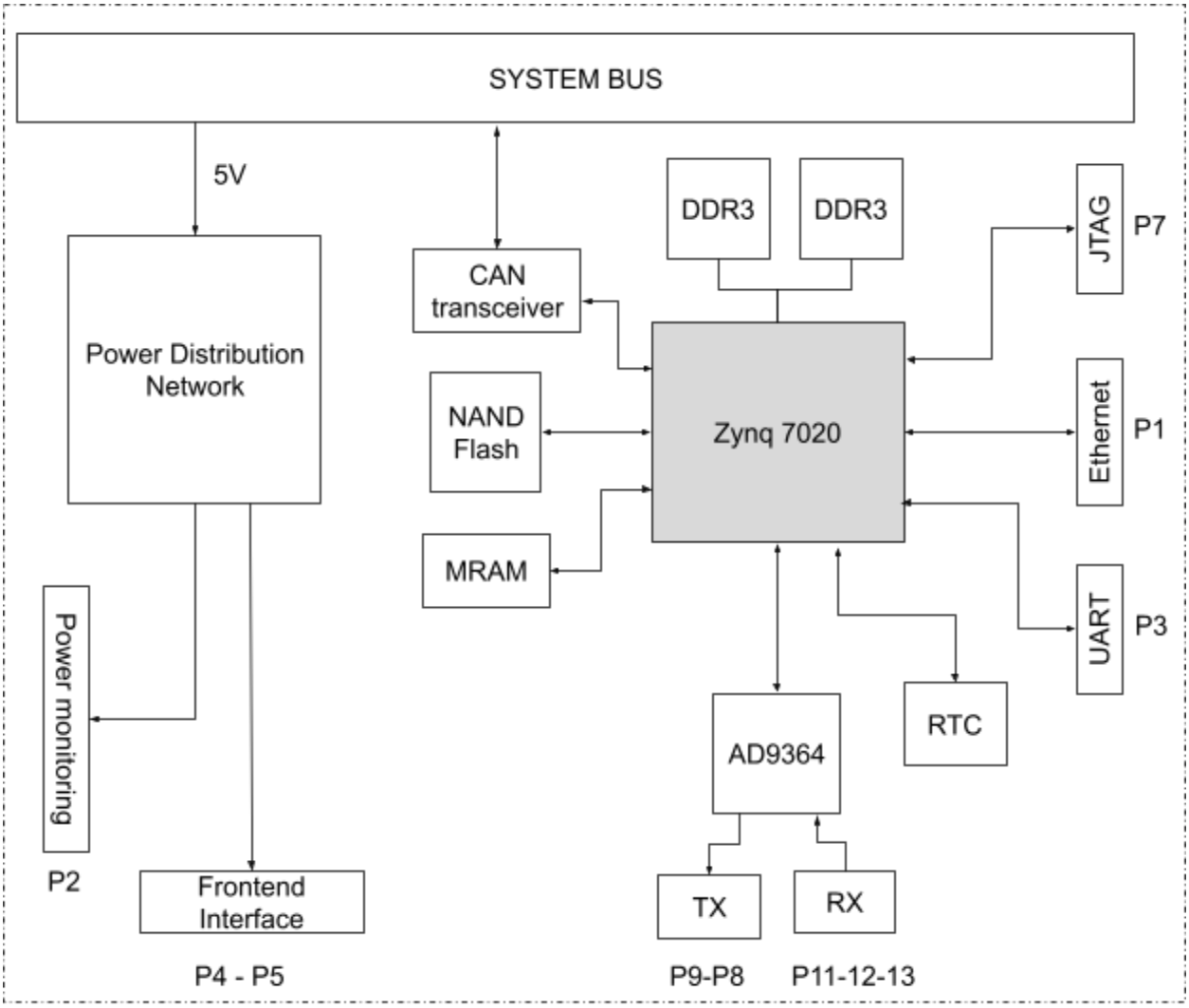

Figure 1: TOTEM-Motherboard block diagram.

3 Functional Description

3.1 System Bus

The system bus is the connector that allows to stack TOTEM in the satellite platform, according to the PC104 Space standard. Through the system bus, TOTEM receives power (5V) and has means of communications such as CAN and I2C.

3.2 Power Distribution Network

The TOTEM-Motherboard has its own power distribution network. Its purpose is to generate and distribute the different voltages and currents required by both TOTEM-Motherboard and the RF frontend.

3.3 NAND Flash

The NAND Flash memory stores the different software images and has 8GB of capacity.

3.4 DDR3L

A total of 1GB of DDR3L memory is available (512 MB with ECC).

3.5 Zynq-7020

The TOTEM-Motherboard core is based on a Zynq-7020, a Xilinx System On Chip (SoC) of the family Zynq-7000 All Programmable SoC. This SoC is divided in two parts: The Processing System (PS) based on a dual ARM Cortex-A9 and the Programmable Logic (PL) which contains 85K logic cells with dedicated DSP slices. These two parts are merged on a single device providing the flexibility of software programmability as well as hardware acceleration implemented on the FPGA.

The Linux operating system is installed in the TOTEM-Motherboard.

3.6 AD9364

The AD9364 is a highly integrated RF transceiver. It operates in the 70 MHz to 6.0 GHz range with a tunable channel bandwidth of 200 KHz to 56 MHz, covering most of the licensed and unlicensed bands.

In transmission, the AD3964 will filter and upconvert the data received by the Zynq-7020. In reception, the AD9364 will filter and downconvert the data received by the RF frontend and send it to the Zynq-7020.

Also the AD9364 has 2 differential transmitters and 3 differential receivers. The TX outputs are connected to the RF frontend through a cable from the TOTEM-Motherboard (P9-P11 connectors). The RX inputs are connected to the TOTEM-Motherboard through a RF cable from the RF frontend (P11 to P13 connectors).

The communication interface between the Zynq-7020 and the AD9364 is over a 12 bit LVDS interface (6 bit TX differential input bus with internal LVDS termination and 6 bit RX differential output bus with internal LVDS termination).

3.7 RF frontend interface

The RF frontend interface has two FSI connectors that allow for easy piggy-backing of the RF frontend board with the TOTEM-Motherboard. Through this interface, the TOTEM-Motherboard will supply power and control the RF frontend. A variety of custom frontends can be attached to the motherboard following the RF frontend interface. (Check Alén Space frontends portfolio).

3.8 Housekeeping

A complete housekeeping system is hardware implemented to monitor all currents, voltages and temperatures in both the PCB and within the SoC, allowing the user to fully control and monitor any anomaly or bad functioning of the entire board.

4 Power Supply

The Power Distribution Network (PDN) is in charge of generating and distributing the power needs for the different parts in TOTEM-Motherboard. The PDN is formed by all the power regulators, the reset

circuit and the power planes that deliver the energy to each device on a specific sequence at power up. The different voltages required by TOTEM-Motherboard are as follows:

- 0V95
- 1V3
- 1V8
- 1V35
- 2V5
- 3V3

Due to the strict power up requirement of the Zynq-7020 SoC, the power distribution needs to be properly sequenced as described in the diagram.

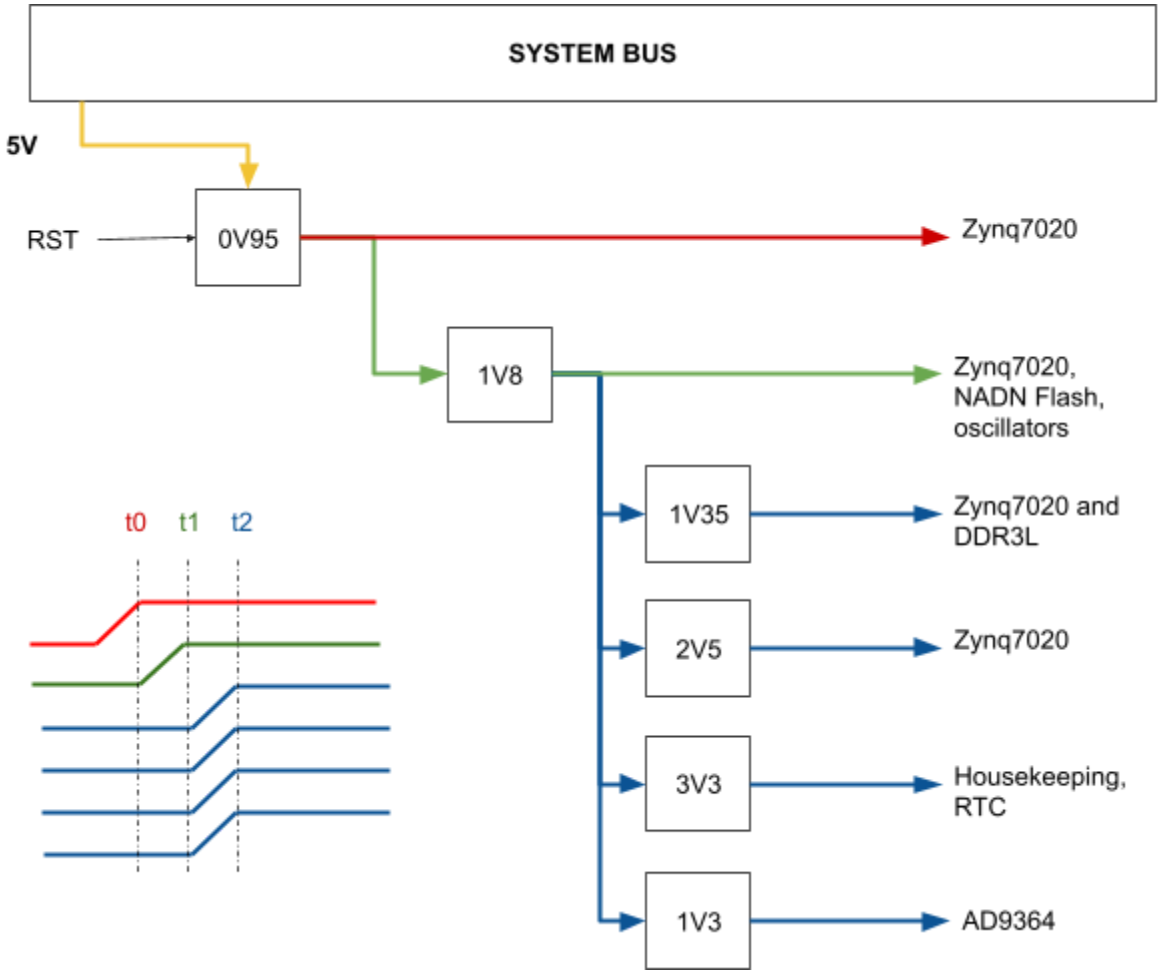

Figure 2: Power distribution network.

4.1 Reset system

The TOTEM-Motherboard is able to reset itself in case of an anomaly detection. To achieve this, a dedicated reset pin in the Zynq-7020 is connected to the reset system that disconnects the power chain for 190 ms, leaving TOTEM completely unpowered. Following that 190 ms gap, the power up sequence initializes.

5 Connectors

5.1 Connectors layout

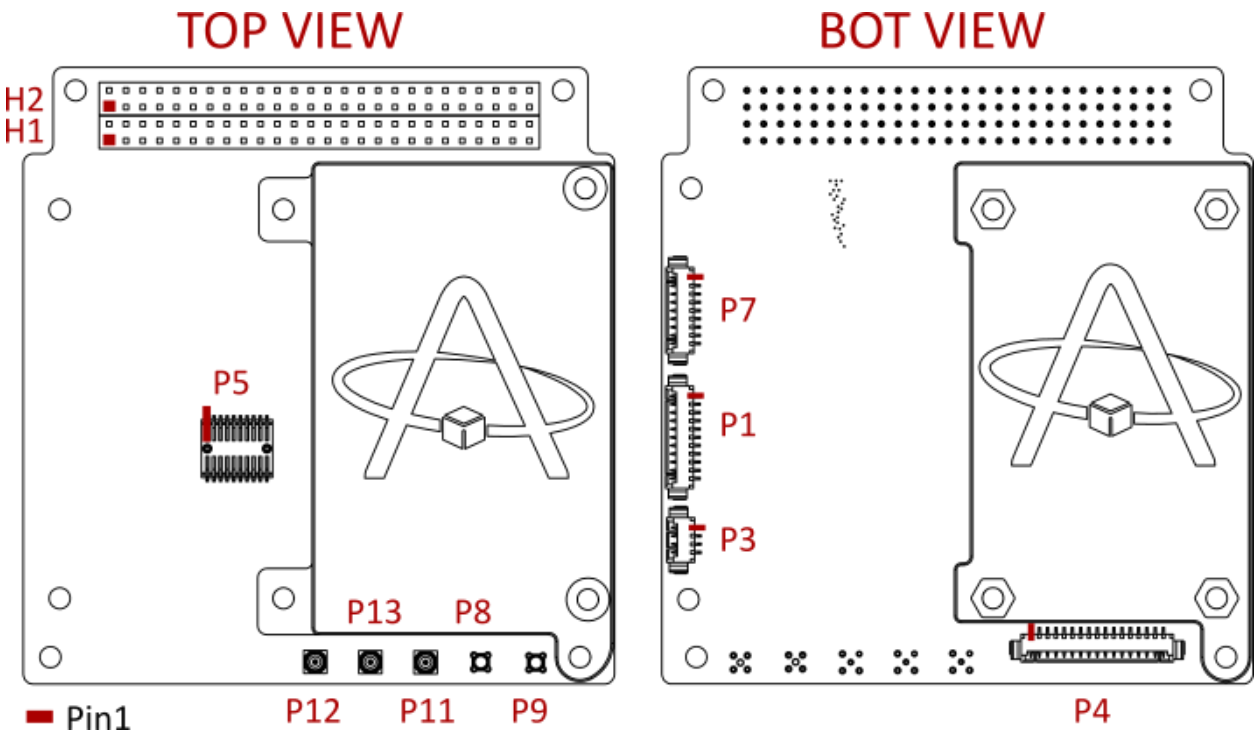

Figure 3: TOTEM-Motherboard top and bottom connectors layout.

5.2 Connectors pinout

5.2.1 System Bus

This connector is used to provide access to the satellite platform. It is composed of two 2x27-pin SSQ (SSQ-126-04-G-D) from Samtec. Other compatible connectors can be selected.

Table 2 - H1/H2 pinout

H1		H2	
Pin	**Description**	**Pin**	**Description**
1	CANL	29	GND
3	CANH	30	GND
37	EXT_GPIO1_3V3[1]	31	GND
39	EXT_GPIO0_3V3[1]	32	GND
41	SDA		
43	SCL		
45	EXT_GPIO2_3V3[1]		
52	VCC 5V		

Note1: General purpose input/output pins connected to SoC (FPGA) 3V3 bank. By default they are not connected.

5.2.2 P1 - Ethernet

Through the ethernet connector you can use an external ethernet module such as the Waveshare DP83848 and connect it according to the following interface.

Logic levels are 3.3V.

The connector is a 11-pin picoblade (53261-7011) from Molex.

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Table 3.- P1 pinout

Pin	Name	Description
1	3V3	Power supply generated by TOTEM-Motherboard
2	MDIO	Management data I/O
3	MDC	Management Data Clock
4	OSC_IN	Oscillator input
5	CRS_DV	Carrier Sense/Receive Data Valid
6	RX0	Receive data
7	RX1	Receive data
8	TX_EN	TX_EN
9	TX0	Transmit data
10	TX1	Transmit data
11	GND	Ground

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5.2.3 P3 - UART

The UART Debug connector is a 4-pin picoblade (53261-0471) from Molex.

Table 5 - P3 pinout

Pin	Name	Description
1	GND	Ground
2	N.C	Not connected
3	RX (Input)	UART RX (3V3 Level)
4	TX (Output)	UART TX (3V3 Level)

5.2.4 P4 - Frontend Interface (Molex)

P4 connector is an external interface to control an external frontend. It is designed to work with Alen Space frontends. There is another frontend interface (P5), with the same signals that allows to connect a frontend as a piggyback board, instead through cable (P4).

The P4 connector is a 17-pin molex picoblade (53261-1771).

Table 6 - P4 pinout

Pin	Name	Description
1	FE_AN_IN1	Analog read[1]
2	FE_AN_IN0	Analog read[1]
3	FE_GPIO1_3V3	General purpose pin I/O (3V3 level)
4	FE_GPIO0_3V3	General purpose pin I/O (3V3 level)
5	FE_GPIO2_2V5	General purpose pin I/O (2V5 level)
6	FE_GPIO3_2V5	General purpose pin I/O (2V5 level)
7	FE_AN_OUT1	Digital to Analog converter from AD9364 CH1 (0 to 3V3)
8	FE_AN_OUT0	Digital to Analog converter from AD9364 CH2 (0 to 3V3)

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9	FE_GPIO0_2V5	General purpose pin I/O (2V5 level)
10	GND	Ground
11	GND	Ground
12	VCC3V3	3V3 power supply
13	VCC3V3	3V3 power supply
14	GND	Ground
15	GND	Ground
16	VCC5V0	5V power supply
17	VCC5V0	5V power supply

Note1: These lines are connected to a voltage divider to protect the xADC. **The user must never exceed 2V input in these lines.**

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5.2.5 P5 – Frontend Interface (FSI)

The P5 connector is a 2x10-pin FSI (FSI-110-03-G-D-AD) from Samtec.

Table 7 - P5 pinout

Pin	Name	Description
1	VCC3V3	3V3 power supply
2	VCC3V3	3V3 power supply
3	GND	Ground
4	GND	Ground
5	VCC5V0	5V power supply
6	VCC5V0	5V power supply
7	GND	Ground
8	GND	Ground
9	GND	Ground
10	GND	Ground
11	FE_AN_IN1	Analog read[1]
12	FE_AN_IN0	Analog read[1]
13	FE_GPIO1_3V3	General purpose pin I/O (3V3 level)
14	FE_GPIO0_3V3	General purpose pin I/O (3V3 level)
15	FE_GPIO3_2V5	General purpose pin I/O (2V5 level)
16	FE_GPIO2_2V5	General purpose pin I/O (2V5 level)
17	FE_GPIO1_2V5	General purpose pin I/O (2V5 level)
18	FE_GPIO0_2V5	General purpose pin I/O (2V5 level)

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19	FE_AN_OUT1	Digital to Analog converter from AD9364 CH1 (0 to 3V3)
20	FE_AN_OUT0	Digital to Analog converter from AD9364 CH2 (0 to 3V3)

Note1: These lines are connected to a voltage divider to protect the xADC. **The user must never exceed 2V input in these lines.**

5.2.6 P7 - JTAG

Connector used for on ground programming and debugging through JTAG. It is a 4-pin picoblade (53261-0971) from Molex.

Table 8 - P7 pinout

Pin	Name	Description
1	Vref	Voltage reference provided by TOTEM-Motherboard
2	TMS	JTAG Test mode select
3	BOOT config	Boot configuration : Connect to GND to enable JTAG boot or leave it open for NAND Flash boot mode.
4	TCK	JTAG Test Clock
5	GND	Ground
6	TDO	JTAG Test Data Out
7	GND	Ground
8	TDI	JTAG Test Data In
9	PS_RST	Reset

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5.2.7 P8/P9 - TX RF connector

MMCX RF transmission connectors (73415-1471) from Molex.

Table 10 - P8 and P9 pinout

Pin	Description
1	TX RF output signal
2	GND

5.2.8 P11/P12/P13 - RX RF connector

MMCX RF reception connectors (73415-1471) from Molex.

Table 11 - P11/P12/P13 pinout

Pin	Description
1	RX RF input signal
2	GND

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6 Data Interface

6.1 CAN Bus

The TOTEM-Motherboard has a CAN Bus interface routed to the system bus, allowing the communication with the TOTEM-Motherboard to be compatible with CSP (Cubesat Space Protocol) packets.

CSP source code: https://github.com/libcsp/libcsp

6.2 UART

An UART interface is available for debugging through connector P3. The Logic level is 3,3V.

6.3 JTAG

The JTAG interface is accessible from the P7 connector and can be used with the Platform Cable USB II from Xilinx. This USB platform provides integrated firmware (hardware and software) to deliver high-performance, reliable and easy-to-perform configuration of Xilinx devices'

Xilinx Platform Cable USB II datasheet:
https://www.xilinx.com/support/documentation/data_sheets/ds593.pdf

6.4 Ethernet

An RMII interface is configured to be accessible from connector P1. An ethernet transceiver such as the DP83848 can be connected on this port to gain network access to the SoC.

The use of such an external device may raise the current consumption of TOTEM. Make sure that absolute maximum ratings are not exceeded for proper operation.

7 Electrical characteristics

Table 14 - Electrical characteristics

Symbol	Description	Min	Typ	Max	Unit
Vcc	Supply voltage	4.7	5	5.2	V
I	Supply current	[1]	0.28	0.53 [2]	A
Pmax	Maximum power consumption	-	1.4	2.62	W

Notes:

1. Minimum current supply when power up may rise to 0.5 A.
2. Maximum current consumption in transmission mode at maximum values: 7 dBm output ,BW = 56 MHz and 30 MSPS

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8 Absolute maximum ratings

Remarks:

- This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied.
- Operating beyond the maximum ratings for extended periods of time may affect product reliability and cause permanent damage.

Table 15 - Absolute maximum ratings

Symbol	Description	Min	Max	Unit
Vcc	Supply voltage	3.7	6	V
VBAT	Unregulated line maximum voltage	-	26	V
Icc	Supply current	-	3	A
Temp	Operating Temperature range	-40	+85	ºC

9 Physical characteristics

Table 16 - Physical characteristics

Magnitude	Value	Unit
Size	93.3 x 89.3 x 5	mm
Mass (shielding not included)	59	g
Mass (shieldings included) [1]	130	g

Notes :

1. Shieldings in both TOP (over SoC and transceiver) and BOT (power supply chain) layers

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9.1 Mechanical drawings

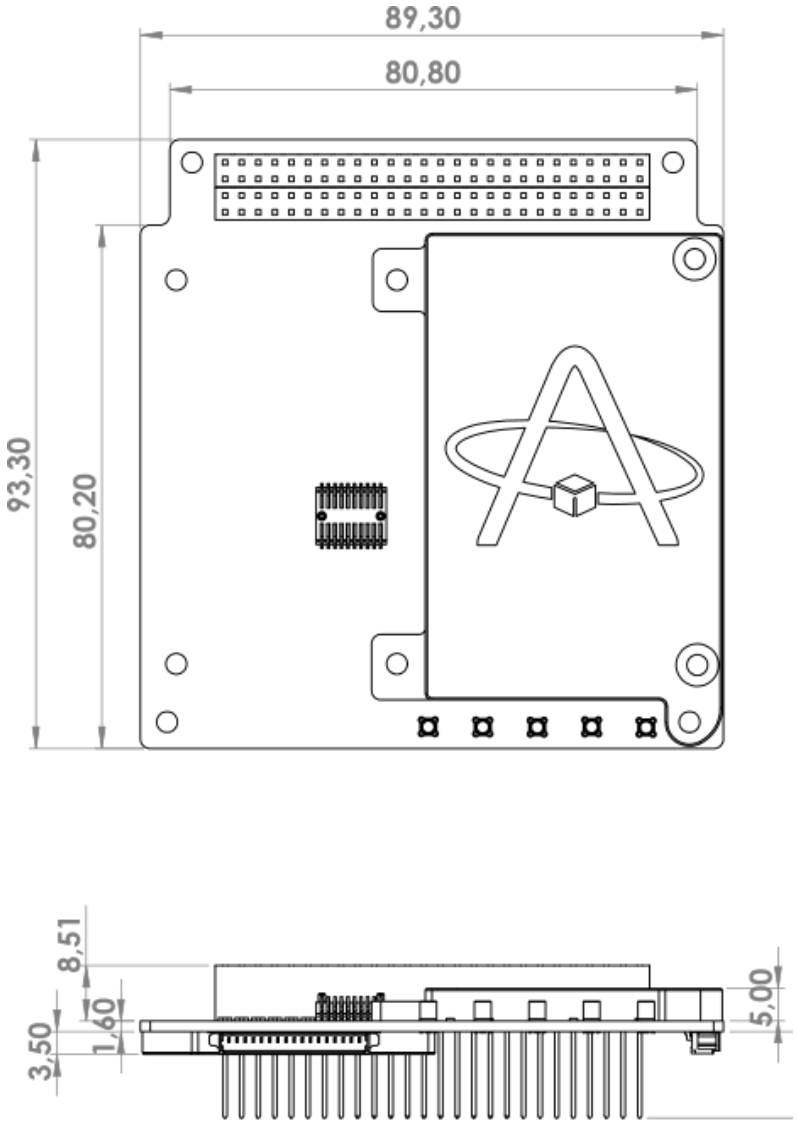

Figure 4 : Mechanical drawings

Note: Stack bus connector pins height depend on the chosen part number